

**HYBRID SYNTHESIZER BASED ON PHASE-LOCK LOOP (PLL) DRIVEN
DIRECT DIGITAL SYNTHESIZER (DDS)**

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**HYBRID SYNTHESIZER BASED ON PHASE-LOCK LOOP (PLL) DRIVEN
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by

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TABLE OF CONTENTS

	Page
ACKNOWLEDGMENTS	ii
TABLE OF CONTENTS	iii
LIST OF TABLES	vi
LIST OF FIGURES	vii
LIST OF SYMBOLS AND ABBREVIATIONS	ix
ABSTRAK	xi
ABSTRACT	xii
CHAPTER ONE: INTRODUCTION	
1.1 Overview	1
1.2 Problem statement	7
1.3 Objectives	7
1.4 Research scope	8
1.5 Significance of research	8
1.6 Thesis organization	9

	Page
 CHAPTER TWO: LITERATURE REVIEW	
2.1 Overview	10
2.2 Hybrid Synthesizers	10
2.3 Phase noise of Hybrid Synthesizers	13
2.4 Switching speed of Hybrid Synthesizers	17
2.5 Spectral purity of Hybrid Synthesizers	20
2.6 Summary	23
 CHAPTER THREE: RESEARCH METHODOLOGY	
3.1 Overview	24
3.2 Phase-Lock Loop (PLL) Synthesizer	25
3.3 Direct Digital Synthesizer (DDS)	30
3.4 Proposed PLL driven DDS Hybrid Synthesizer	34
3.5 Hybrid Synthesizer Phase Noise Measurement	40
3.5.1 Three-oscillator comparison	40
3.5.2 Two-oscillator comparison	42
3.6 Hybrid Synthesizer Switching Speed Measurement	43
3.7 Hybrid Synthesizer Spectral Purity Measurement	46
3.8 Summary	49

	Page
CHAPTER FOUR: RESULTS AND DISCUSSIONS	
4.1 Overview	50
4.2 Phase noise results	50
4.3 Switching speed results	54
4.3.1 Normal mode switching speed	54
4.3.2 Fast continuous wave switching (FCWS) speed	57
4.4 Spectral purity results	59
4.4.1 Harmonics	60
4.4.2 Subharmonics	62
4.4.3 Spurious	66
4.5 Summary	68
CHAPTER FIVE: CONCLUSION AND RECOMMENDATIONS	
5.1 Conclusion	69
5.2 Recommendations	71
REFERENCES	72
APPENDICES	78

LIST OF TABLES

		Page
Table 3.1	E8257D PLL Synthesizer Frequency Generation	29
Table 3.2	N5193A DDS Frequency Generation	34
Table 4.1	Phase noise frequencies and respective regions	51
Table 4.2	Start and stop frequency points for normal mode Switching speed	54
Table 4.3	Harmonics number and frequency measured	60
Table 4.4	Subharmonics number and frequency measured	62
Table 4.5	Proposed hybrid synthesizer vs. standalone DDS synthesizer.	68

LIST OF FIGURES

	Page
Figure 1.1 Phase-lock loop (PLL) block diagram. [1]	2
Figure 1.2 Lock and Unlock condition of a PLL. [5]	4
Figure 1.3 Direct Digital Synthesizer (DDS) block diagram. [8]	5
Figure 1.4 The phase and waveform advance concept for DDS. [9]	5
Figure 2.1 DDS-PLL based frequency synthesizer. [12]	11
Figure 2.2 Hybrid synthesizers. [13]	12
Figure 2.3 Block diagram of hybrid Synthesizer based on PLL with DDS in the feedback. [20]	15
Figure 2.4 Block diagram of hybrid synthesizer based on DDS-driven PLL. [20]	16
Figure 2.5 Block diagram of hybrid synthesizer based on PLL with DDS-generated frequency offset. [20]	16
Figure 3.1 PLL Synthesizer E8257D PSG Signal Generator. [35]	25
Figure 3.2 E8257D PSG Block Diagram. [35]	26
Figure 3.3 20 GHz Doubler Circuitry. [35]	29
Figure 3.4 DDS Synthesizer N5193A UXG Signal Generator. [36]	30
Figure 3.5 N5193A UXG Block Diagram. [36]	31
Figure 3.6 Frequency generation process of the proposed system.	38
Figure 3.7 Block diagram of the proposed system.	39

		Page
Figure 3.8	Phase noise measurement setup.	43
Figure 3.9	Switching Speed Measurement Setup.	44
Figure 4.1	Phase noise at carrier frequency of 11399 Hz	52
Figure 4.2	Normal Mode Switching at Start Frequency 15000 MHz	57
Figure 4.3	FCWS Switching at Start Frequency 15000 MHz.	59
Figure 4.4	2nd Harmonics across frequency 10 to 10000 MHz	61
Figure 4.5	Harmonics across frequency 10 to 6000 MHz	61
Figure 4.6	Subharmonics number at 0.2500	63
Figure 4.7	Subharmonics number at 0.3750	63
Figure 4.8	Subharmonics number at 0.5000	64
Figure 4.9	Subharmonics number at 0.7500	64
Figure 4.10	Subharmonics number at 1.250	65
Figure 4.11	Subharmonics number at 1.5000	65
Figure 4.12	Reference spurs between 10 MHz to 20 GHz	67

LIST OF SYMBOLS AND ABBREVIATIONS

PLL	-	Phase Lock Loop
DDS	-	Direct Digital Synthesizer
Hz	-	Hertz
kHz	-	Kilohertz
MHz	-	Megahertz
GHz	-	Gigahertz
PXIe	-	PCI eXtensions for Instrumentation express
CW	-	Continuous Wave
IF	-	Intermediate Frequency
RF	-	Radio Frequency
LO	-	Local Oscillator
DAC	-	Digital-to-Analog Converter
dB	-	Decibels
dBm	-	Decibels (dB) of power referenced to one milliwatt (mW).
dBc	-	Decibels relative to the carrier
SFDR	-	Spurious-Free Dynamic Range
WIFI	-	Wireless Fidelity
VCO	-	Voltage Control Oscillator
DRO	-	Dielectric Resonator Oscillator
SAW	-	Surface Acoustic Wave
YIG	-	Yttrium-Iron-Garnet
WLAN	-	Wireless Local Area Network
W-CDMA	-	Wideband Code Division Multiple Access
FPGA	-	Field-Programmable Gate Array
Frac-N	-	Fractional-N
DUT	-	Device Under Test

UUT	-	Unit Under Test
FCWS	-	Fast Continuous Wave Switching
RBW	-	Resolution Bandwidth
EMI	-	Electromagnetic Interference
<i>TwoOsc.</i>	-	Two-Oscillator Comparison
<i>REF</i>	-	Noise from the reference source of three oscillator comparison
t_{f1}	-	Time when the hybrid synthesizer settled at stop frequency
t_{stop}	-	The actual stop time
t_{cap}	-	The signal analyzer/oscilloscope capture time
t_{rep}	-	Repeatability variances

PENSINTESIS HIBRID BERDASARKAN GELUNG TERKUNCI FASA (PLL) DIDORONG PENSINTESIS DIGITAL LANGSUNG (DDS)

ABSTRAK

Pembangunan pensintesis frekuensi telah berkembang saban tahun dari model yang besar kepada model yang kompak mudah alih dan yang terkini berbentuk modular. Oleh kerana perkembangan teknologi yang pesat terutama dalam industri telekomunikasi dan sistem pertahanan ketenteraan, permintaan pensintesis frekuensi yang berprestasi tinggi semakin meningkat. Kajian ini membincangkan mengenai penggabungan antara fasa kunci gelung (PLL) dan pensintesis digital langsung (DDS) menjadi sebuah system hibrid PLL didorong DDS. Kajian ini teretus kerana kekurangan informasi dan kerja-kerja penyelidikan mengenai prestasi sistem hibrid seperti ini. Malah, melalui penggabungan dua struktur pensintesis menjadi sistem hibrid mampu mengatasi kekangan yang dihadapi oleh pensintesis yang berdiri bersendirian. Prestasi yang dinilai ialah seperti hingar fasa, kelajuan pensuisan dan ketulenan spektra dan keputusan yang diperolehi telah dibandingkan dengan DDS. Peningkatan prestasi hanya ditunjukkan untuk kelajuan pensuis mod FCWS. Manakala terdapat degradasi untuk prestasi seperti hingar fasa, sub harmonik dan rujukan palsu. Keputusan harmonik dan kelajuan pensuisan mod biasa di antara dua sistem adalah sama. Walaupun sistem yang dicadangkan mempunyai beberapa kelemahan, tetapi prestasi yang ditunjukkan oleh sistem tersebut masih mampu beroperasi untuk aplikasi yang berprestasi tinggi. Terdapat banyak peluang dan kerja-kerja penambahbaikan yang boleh dibuat supaya menjadi salah satu reka bentuk yang terbaik yang terdapat di pasaran sekarang.

HYBRID SYNTHESIZER BASED ON PHASE-LOCK LOOP (PLL) DRIVEN DIRECT DIGITAL SYNTHESIZER (DDS)

ABSTRACT

Throughout the years, the development of a frequency synthesizer has evolved from large and heavy benchtop models to the compact size handheld synthesizer and now in modular form. Due to the fast-growing technology in wireless telecommunication industries and high expenditure or budget allocation to improve the military and defense system, the frequency synthesizer has become one of the highest demand instruments in the market now. The research will focus on conventional Phase-Lock Loop (PLL) and latest technology of Direct Digital Synthesizer (DDS) and combine to become a hybrid PLL driven DDS synthesizer. This research was triggered since there was minimum work that has been covered and undetermined performances for such hybrid design. Furthermore, the problems faced for standalone synthesizers can be overcome through the hybrid system design. Phase noise, switching speed and spectral purity was the performance evaluated for the proposed setup and was compared with a standalone DDS synthesizer. Results shows the FCWS switching speed improved but there was degradation seen on phase noise and spectral purity particularly on the subharmonics and reference spurious. The harmonics and normal mode switching speed shows no difference between both systems. Although there was some performance degradation observed, the proposed setup performances are still under specifications for high performances applications and there are rooms for future improvement to be one of the best synthesizer designs that the market could offer.

CHAPTER 1

INTRODUCTION

1.1 Overview

A signal generator is an instrument that produces sine waves. It can perform numerous measurements that cover a wide band of frequencies to cater industries like electronics warfare, aerospace defense, and wireless communication. The development works on a signal generator from bench-top or PXIe modular models to the portable hand-held concept are still on-going to ensure customer demands and requirements are being met.

As time moves forward, the signal generator has evolved from a basic continuous wave (CW) signal generator to the latest analogue and vector signal generator that offers various type of modulation. Modulation is one of the important characteristics of a signal generator as it is a process of generating a new signal through signal mixing process. A CW signal generators that produce output less than 6 GHz are commonly referred as radio frequency (RF) range of signals. Whereas an analogue or a vector signal generator that has the capability to produce signals greater than 30GHz are known as microwave signals.

The main component of the signal generator in producing sine waves is called a synthesizer. There are several architectures of synthesizer that have been developed throughout the years but this research had focused on indirect conventional phase-lock loop (PLL) synthesizer and direct digital synthesizer (DDS). The PLL synthesizer consist of elements such as the reference signal, a phase comparator or detector, an amplifier, a loop filter and a voltage control oscillator (VCO) shown in Figure 1.1.

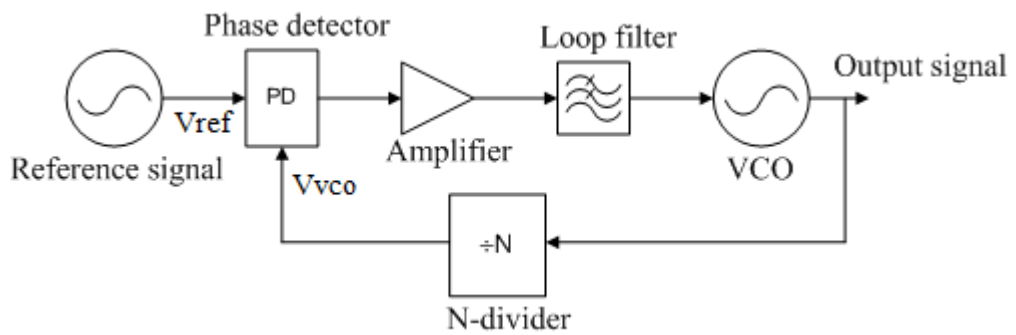


Figure 1.1: Phase-lock loop (PLL) block diagram. [1]

A signal from the VCO will enter to the phase detector. The VCO should have excellent short-circuit stability, free from harmonics, and have a predictable voltage-to frequency curve to ensure that an increase in voltage always causes an increase in output frequency [2]. Next, the VCO and incoming reference signal phases are compared and produced an error voltage which corresponds to the phase difference between the two signals.

The amplifier located between the phase detector and VCO is mainly to reduce the actual error to a very small level. However, to achieve a correct desired frequency, there must be some voltage present at the control terminal of the VCO. The PLL in the feedback functions as the noise filter and calibrates the phase error [3].

The error signal will pass through the loop filter circuit which acts as a low pass filter to remove the unwanted high frequency elements in the signal. The signal that comes out from the loop filter will be the tuning voltage for the VCO. The sense of any change in this voltage is such that it tries to reduce the phase difference and frequency between the two compared signals.

At first, the loop will be in out of lock condition and the error voltage will pull the VCO frequency to match with the reference until the error is small. At this moment, the PLL is in lock condition and a steady state error voltage is produced. As the steady state error voltage is present, the phase difference between the reference and the VCO is not changing which also means that both signals are in the exact same frequency.

Figure 1.2 shows an example of lock and unlock condition for a PLL measured at the phase detector which corresponds to the phase difference between the VCO signal and the reference signal. Fractional-N PLLs are preferred as frequency synthesizers due to their wide bandwidth and fine frequency resolution [4].

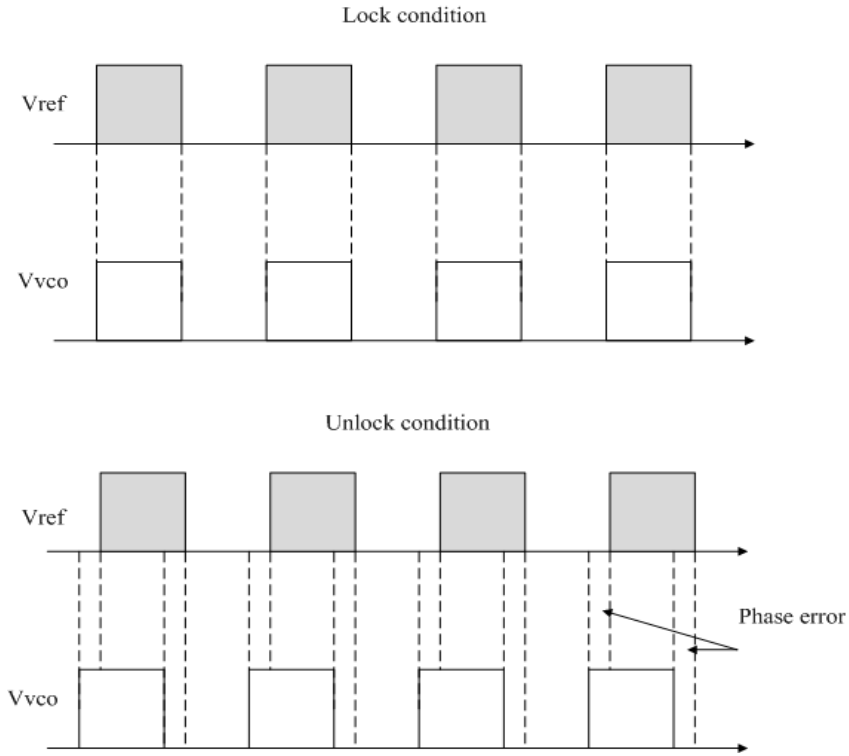


Figure 1.2: Lock and Unlock condition of a PLL. [5]

As the demand for high performance synthesizer grew, newer technologies such as the DDS technique was developed. This technique has the capability of generating frequency and phase agile local oscillator (LO) source that could outperform the conventional PLL especially in areas such as frequency resolution and switching speed.

The concept of the DDS is especially suitable for the lower microwave region down to frequencies of few kHz or MHz [6]. Apart from that, DDS integrated circuits (IC) support to generate precise linear frequency modulation signals up to several hundred megahertz [7]. However, if the DDS is directly used as a LO, there will be problems in terms of spurious generation which modern transceivers could not accept.

The main components of a simple DDS are phase accumulator, waveform map (ROM or PROM) and a digital-to-analog (DAC) converter as shown in Figure 1.3. It operates by storing and recalling points of waveforms in digital format to produce a full cycle of analog waveform. The concept used in a DDS is explained through the phase advances around a circle which corresponds to the advances of the waveform as shown in Figure 1.4.

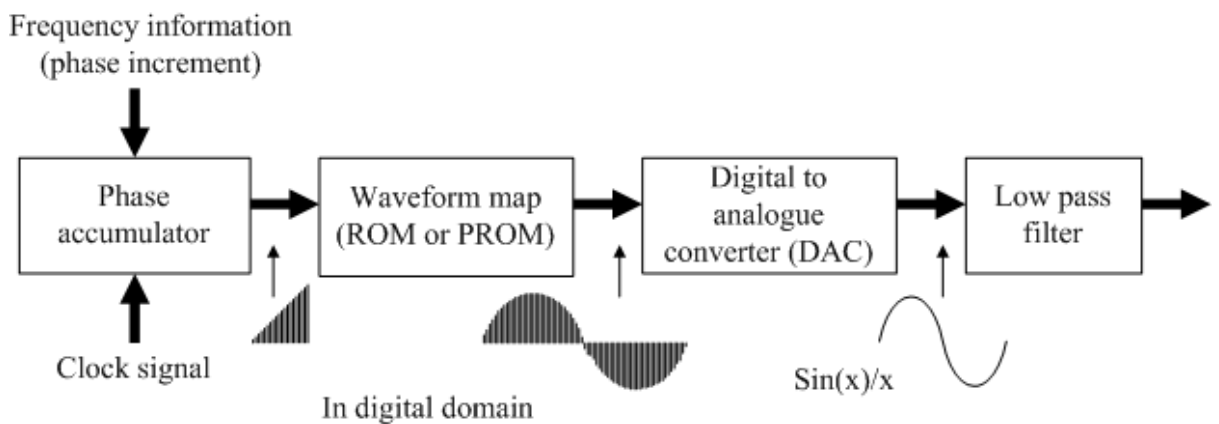


Figure 1.3: Direct Digital Synthesizer (DDS) block diagram. [8]

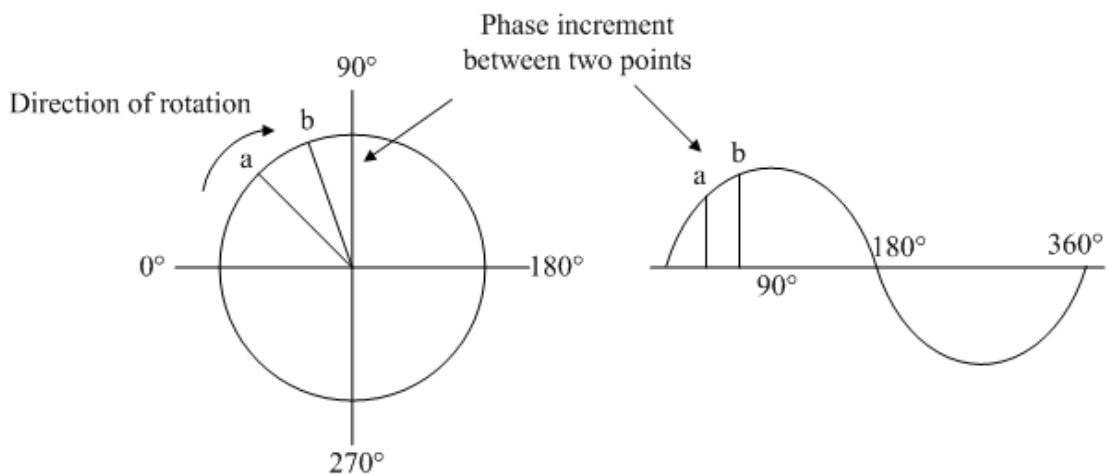


Figure 1.4: The phase and waveform advance concept for DDS. [9]

A certain number of digital bits that represent the phase of a waveform are held at the phase accumulator. This phase accumulator which acts as a counter will count the number of digital bits which increased at regular intervals. Once the accumulator is filled up, the counting process will reset and start from zero again.

The process of converting the digital representation of the waveform is done once the phase has been determined through the waveform map also known as the sine look-up table. This memory map can either be a read-only memory (ROM) or a programmable read-only memory (PROM) stores a number that corresponds to the required voltage for each value of phase in the waveform.

Next, a digital to analog (DAC) converter is used to convert the digital numbers from the sine look-up table into an analogue voltage. This waveform then will go through a low pass filter to remove the unwanted signals and to give the desired level as necessary. The phase truncation process performed by the DDS will cause high output spurious of the system [10]. Hence, the phase truncation error needs to be small as possible to improve the spurious performance.

The DDS tuning is achieved through the step or phase increment between different sample points. To achieve a high frequency which also means that phase reaches a full cycle faster, a larger increment update is done to the phase accumulator. Using smaller increment to the phase accumulator will result in a longer time to reach a full cycle which corresponds to a low value of frequency. The frequency change can be made instantly by changing the increment value and the frequency resolution is determined by the number of points in the accumulator.

1.2 Problem Statement

The trend of demands for high performance synthesizer especially for industries like military and defense, radar, wireless and telecommunication has increased and standalone synthesizer, either a PLL or DDS, has its own disadvantages. A PLL synthesizer has slower switching speed whereas a DDS synthesizer have problems with harmonics. Thus, the combination of both systems can overcome the problems faced by standalone synthesizer.

The performance of a PLL driven DDS Hybrid Synthesizer is undetermined due to less information and minimum of research works conducted in the past. Hence, this study will explore new findings which bring useful information for signal generator users.

1.3 Objectives

The objectives of this research are:

- i. To investigate a PLL driven DDS Hybrid Synthesizer.
- ii. To implement a hardware realization for the proposed design.
- iii. To evaluate the performance of the designed hybrid synthesizer

1.4 Research scope

In this research, the frequency synthesizers used were confined to the PLL and DDS architecture due to the capability of each system operating for high performance applications. Furthermore, these two architectures have been well established and widely used for frequency generation purposes. Hence, the operating frequency for the proposed system is limited from 10 MHz to 20 GHz which could cater across several industries like telecommunications, military & defense, radar & satellite and many more. The performances assessed are the phase noise, switching speed and spectral purity and will be benchmarked against the performance of a standalone DDS system. This is mainly because the performances of the proposed system were measured at the output of the DDS synthesizer which will follow majority of the DDS characteristics. Detailed design and measurement methodology were given for better understanding.

1.5 Significance of research

The PLL driven DDS Hybrid Synthesizer design is not fully explored by previous researches. Hence, the characteristics and performance of such system will be determined through this research which also brings new findings for frequency synthesizer applications. The relevance of this study is also to offer more insight to readers on the performance of signal source products. Due to the high cost of owning a signal source, consumer must fully understand how the signal source works to achieve optimum performance which corresponds with their application. Apart from

that, this research will share more on latest technology used in modern synthesizer in preparation for the upcoming fifth generation wireless system also known as 5G.

1.6 Thesis organization

The remainder of this thesis is organized as follows:

Chapter 2 reviews the development of hybrid synthesizers that have been implemented by previous researches. The chapter also discusses on works that have been done to improve the performance of phase noise, switching speed and spectral purity of a hybrid synthesizer.

Chapter 3 explains the method applied in designing the proposed PLL driven DDS Hybrid Synthesizer. The test methodology of measuring each performance of the designed hybrid synthesizer will be explained as well.

Chapter 4 presents the results obtained from the proposed design. Performance comparison between a standalone DDS synthesizer with the designed hybrid synthesizer will be covered in this chapter.

Chapter 5 concludes the overall achievement of this work. Recommendations are also provided for future works to improve the proposed PLL driven DDS Hybrid Synthesizer.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

The chapter begins with section 2.2 which discusses a brief history of the hybrid synthesizers and its current development. Section 2.3 elaborates more on improving the phase noise of the hybrid synthesizers. As the thesis moves to section 2.4, more about hybrid synthesizer switching speed is covered. Section 2.5 which review the work on improving the spectral purity performance is the final topic discussed in this chapter. Basically, each section starts with a brief introduction to ensure readers have better understanding before moving forward to the subsequent chapters.

2.2 Hybrid synthesizer

Modern synthesizer design for a hybrid topology has been developed to take the advantage of combined strength between a DDS and traditional PLL architecture. The low phase noise, low spurious, high hopping-time and broad band had been the main trends for hybrid synthesizer development [11].

Before the technique became practical, there were tradeoffs for both DDS and PLL such as frequency range and resolution, unwanted spurious outputs, and the overall complexity. Normally, a hybrid synthesizer uses a DDS as a source to provide a clean, stable and tunable reference to the conventional PLL. This DDS driven PLL output derives the tuning precision and stability from the DDS while the frequency range coverage is from the PLL.

An example of a hybrid synthesizer designed by Maletic [12] focused on frequency-hopping spread spectrum applications as depicted in Figure 2.1. The design emphasized on frequency agility to achieve fast PLL acquisition times using dual-loop control scheme. The proposed method provides a better RF carrier frequency performance like low spurious signal, low phase noise, short switching time and high output frequency resolution which makes it suitable for radio frequency (RF) applications. Another advantage of using this scheme is that it can be applied to beyond the operating range covered by the DDS.

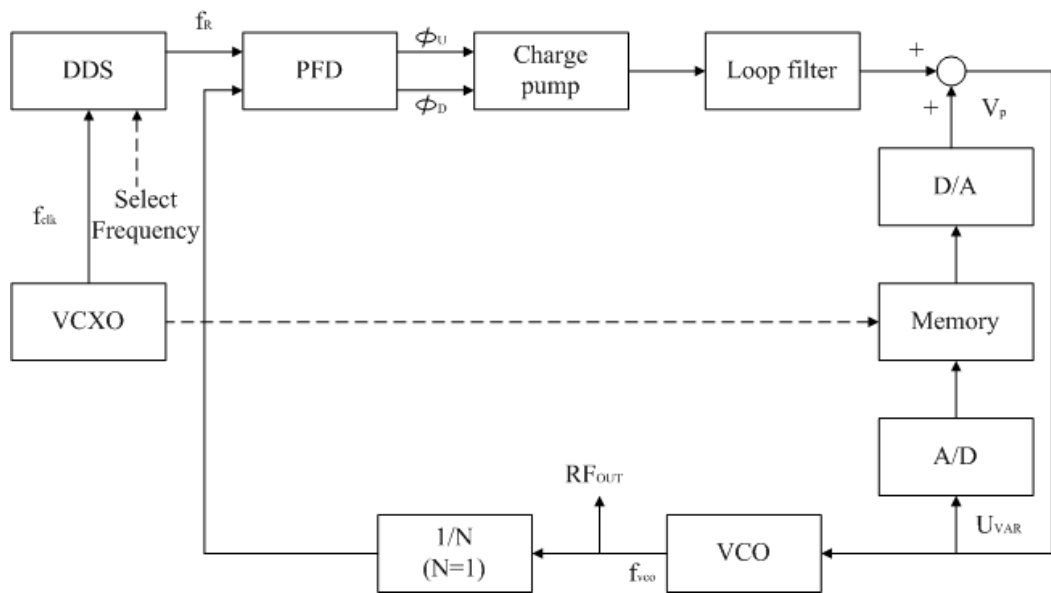


Figure 2.1: DDS-PLL based frequency synthesizer. [12]

The development of hybrid synthesizer by Claerhout and Vandewege [13] which could generate an output frequency ranging from 5 MHz to 500MHz with millihertz (mHz) resolution proves that simple and careful modeling can lead to good overall performance. Basically, the model proposed emphasized on phase noise and tuning speed optimization of such architecture. The system uses a high performance 150MHz crystal oscillator to supply the clock signal for both PLL loop and DDS chip as shown in Figure 2.2.

In contrast to the previous design, this synthesizer make used of the fixed frequency of 196MHz provided by the PLL to mixed with the output of DDS ranging from 1.4GHz to 2GHz to produce the desired output. However, this design which is highly dependent on the crystal oscillator for the clock generation has disadvantages of power drift over time, require tuning or calibration process to ensure a stable signal is provided and the cost is expensive.

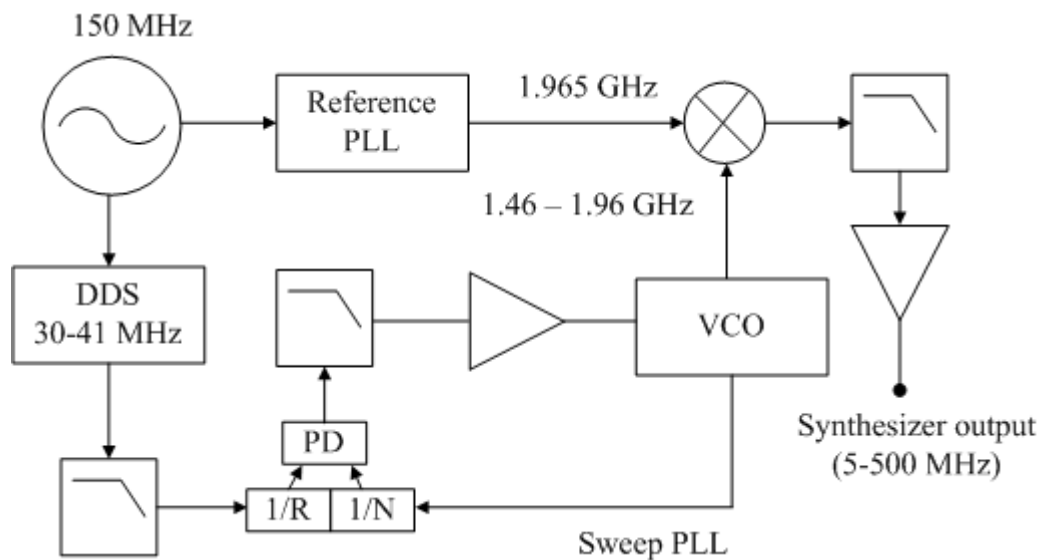


Figure 2.2: Hybrid synthesizers. [13]

Another design method proposed by Miles and Hoskings [14] is closely related to amateur radio and hobbyist sector shares the same goal design as Ben Sneath [15] for a hybrid synthesizer with wide tuning range and fine frequency resolution whilst minimizing the output spurious level. This implementation is based on the similar general architecture as shared in prior examples with the use of a high-performance DDS chip for adjustable reference signal that will be multiplied by a higher frequency at the PLL circuit. Synthesizers that highly rely on high performance DDS chips have problems with spurious signals appearing in their outputs.

Additionally, these high-spec DDS chips consume a substantial amount of power, resulting in excessive heat generation within the circuit [16]. With these characteristics, the overall system becomes undesirable for new transceivers especially for portable or hand-held equipment where power consumption, cost and size are critical factors that need to be considered.

2.3 Phase noise of Hybrid Synthesizer

Phase variations that results in random frequency variation of a signal are the condition to describe the term phase noise. Obtaining a low phase noise LO signal is one of the most significant researches in wireless communication and radar system [17]. In time domain, phase noise can be quantified as jitter. Both phase noise and jitter are the key element in signal generators as they can significantly affect the performance of the system especially in radar and communication industries. Hence,

phase noise levels in the output wave are main parameters that determine the quality of frequency synthesizer [18].

Phase noise can cause loss of sensitivity, lack of definition in imaging process and higher bit error rate in digital system. When designing a synthesizer, it is important to have the phase noise as small as possible, from at least 40 dB to 170 dB less than the carrier. In signal generators, phase noise is measured as the single sideband power referenced to the carrier and the unit is in dBc/Hz.

Phase noise can be divided into two categories which are absolute and residual phase noise. The phase noise measured direct at the RF output of a signal generator is considered as the absolute phase. Once the phase noise of the reference oscillator in the signal generator is subtracted, the amount of phase noise attribute to the system is called residual phase noise.

Works on reducing the phase noise of hybrid synthesizers are still on going by various authors due to the dominant contribution of the noise. Through the usage of passive filtering, the amplitude noise can be addressed effectively but the suppression of spurious phase fluctuations is difficult. The work done by Vasilyev, Kuzichkin, Kurilov and Surzhik [19] on analyzing noise properties of hybrid synthesizer with auto compensating phase noise method has showed that a general relation to investigate noise characteristic together with high efficiency results can be obtained.

The design placed an auto compensator on the DDS and PLL which consist of differentiating circuits, full-wave rectifier and T-flip-flops. By changing the delay of the DDS output signal through the phase shifter controller, the suppression of the noise can be carried out. However, the disadvantage of the proposed method is it has high complexity circuitry with multiple components used to produce such system which directly lead to high power consumption.

The work done by Romashov and Yakimenko [20] on comparing the phase noise of hybrid synthesizer with different configuration between the DDS and PLL has given an insight on how to reduce the phase noise level. The three structures of hybrid synthesizer proposed are depicted in the Figure 2.3 to 2.5. Between these three models, results of the research show that the phase noise level of DDS driven PLL hybrid synthesizer is 5dB/Hz higher compare to other structure. In addition, the research has offered to use the image of DDS output frequency to reduce the phase noise of the hybrid synthesizer by 7-8 dB/Hz.

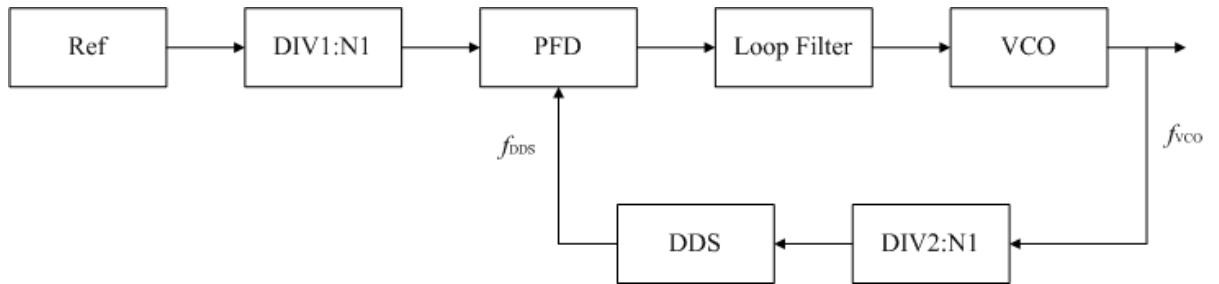


Figure 2.3: Block diagram of hybrid Synthesizer based on PLL with DDS in the feedback. [20]

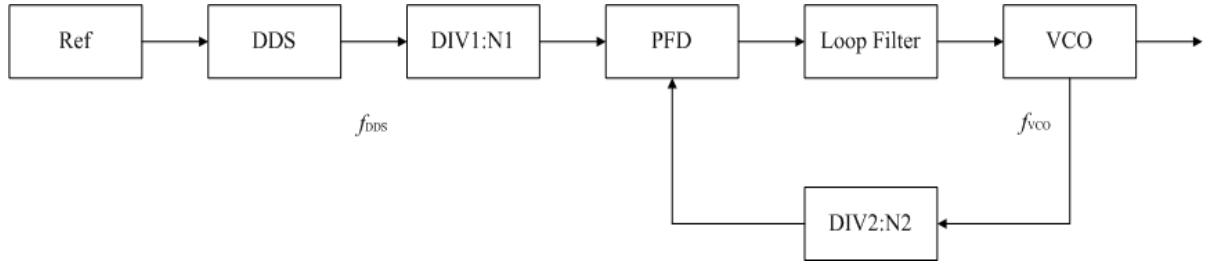


Figure 2.4: Block diagram of hybrid synthesizer based on DDS-driven PLL. [20]

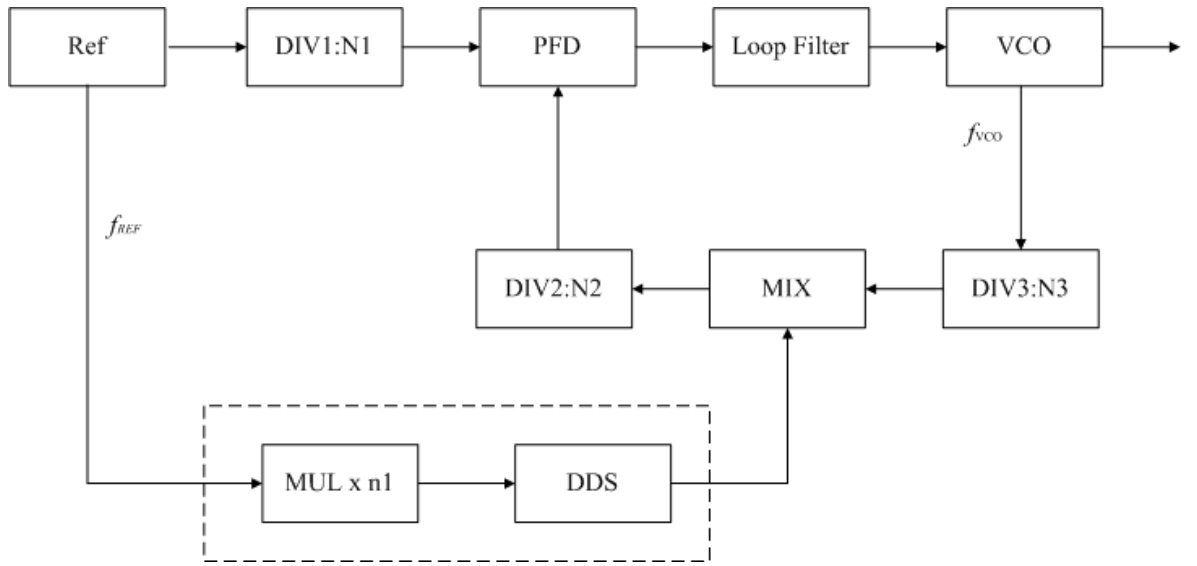


Figure 2.5: Block diagram of hybrid synthesizer based on PLL with DDS-generated frequency offset. [20]

A novel approach of hybrid synthesizer that emphasized on low cost and low phase noise was developed by Ajay and Ulrich [21]. The implemented system has the capability of producing an output frequency up to 10.24 GHz and better phase noise performance than -138 dBc/Hz at 10 kHz offset with noise floor of -174 dBc which are comparable to commercial low cost synthesized signal source available in the market. The improvement of phase noise was achieved by combining a low-noise oven

control crystal oscillator (OCXO) with a low-noise high frequency oscillator such as a dielectric-resonator oscillator (DRO) or surface-acoustic wave (SAW) oscillator.

The close-in performance is determined by the OCXO and harmonic multiplier while the far-offset phase noise performance is determined by the DRO and SAW oscillator. The mixer and loop filter noise performance can be relaxed by 40 dB with the used of reference frequency multiplication technique. Besides the performance of the oscillators, the design uses a low-noise operational amplifier to achieve low phase noise. This design brings advantages such as simple design with small size packaging, high performance over size ratio and the architecture uses low cost components.

2.4 Switching speed of Hybrid Synthesizer

The switching speed performance of a synthesizer depends on the circuit topology and synthesizer technology. If the transition is too soon, the lock speed is slow since the high-speed lock circuit characteristic is not utilized. On the other hand, if the transition is too late, the synthesizer can be unstable or phase noise can be high [22]. Increasing the loop bandwidth is a straightforward way to obtain a fast settling [23].

Indirect PLL synthesizer that uses a VCO or an yttrium iron garnet (YIG) tuned oscillator for frequency generation normally provides slower switching speed in contrast with the DDS synthesizer due to its feedback loop characteristic that requires

certain amount of time to stabilize after a frequency change. Switching speed can be applied both for amplitude or frequency. However, in this research more focus will be put on the frequency switching of a synthesizer since it is a critical performance parameter in many modern communication systems such as Bluetooth technology, WLAN, W-CDMA and 3G [24].

Frequency switching speed or also known as frequency switching time can be defined as the required time for the output of a synthesizer to change from an arbitrary initial frequency to a programmed final frequency [25]. Once the synthesizer receives a switching command, the switching time starts and ends when the phase remains locked to its final frequency. Whenever frequency is synthesized, the waveform generator with the most optimum slope and duration is required. Therefore, the complicated design and the exact synchronization for high-speed switching make it disadvantageous [26].

Soumyadeep [27] has developed a hybrid synthesizer that can produce an output ranging from 6 to 18 GHz wideband frequency with maximum switching time of 6 μ s and spur level less than -50 dBc. To achieve a wide frequency range, the system uses the DDS as a reference to the PLL multiplier. The key factor in producing a fast frequency switching speed synthesizer is by optimizing to a wide loop bandwidth of the overall architecture of the PLL. The combination of frequency settling time and digital processing time is the overall frequency switching time. A fast FPGA that provides the tuning to the PLL, DDS and other components were used to minimize the processing time.

With the use of alternate DDS frequencies and consecutive PLL division ratios, a low spurious noise can be achieved. The advantage of this design is that it can be used as a frequency-agile LO in wideband microwave receivers. However, with the optimization of wide loop bandwidth of the PLL come with a tradeoff whereby the system has insufficient rejection of high close-in DDS spurs by the loop filter. These spurs are generated by the DDS during the phase truncation process which lead to periodic phase error.

As the frequency switching speed is one of the important parameter that impacts the overall system of a synthesizer, Chenakin, Suresh and Iqbal [28] from San Jose, USA has developed a compact and broadband hybrid synthesizer which covers from 0.1 to 10 GHz output frequency with a 0.001 Hz step size. Apart from fast switching speed, the design also covers other characteristics like low phase noise and spurious.

At 10 GHz output frequency, the phase noise measured at 10 kHz offset is -122 dBc/Hz and the spurious performance is less than -70 dB. The design achieved extremely small frequency acquisition time and consequently fast switching speed by ensuring the PLL bandwidth is extended compared to the conventional PLL which uses the same concept as discussed previously. The switching time of the main PLL measured was less than 10 μ s. The advantages of this design are that it can be used as a broadband, agile and high-fidelity signal source for various test and measurement, communication and surveillance systems.

A design developed by Kashif, Malik, Yasin, and Imran [29] that can perform in X-band for radar applications is another example of an agile fast frequency switching hybrid synthesizer. The design uses the digital nature of DDS architecture to obtain the fast frequency switching speed. Four main reasons why the hybrid synthesizer design is capable of having fast frequency switching is due to the phase detector follows changes in reference signal more rapidly, the DDS changes the reference of the PLL very fast, the DDS does not require to load the counter with a new value and the counter does not reset.

2.5 Spectral Purity of Hybrid Synthesizer

Producing a carrier frequency through mixing or dividing process will create non-random or deterministic signals. If the signals are harmonically related to the carrier, these signals are called as subharmonics. On the other hand, non-harmonic spectral lines are called spurious. The unit for subharmonics and spurious are in amplitude related to the carrier or also known as dBc.

The goal is to eliminate these spectral issues but if they cannot be eliminated, then they should be attenuated as much as possible [30]. As critical as phase noise, spurious signals can cause the same problem as well. If a high spurious signal exists, the chances of measuring the wrong signal will occur.

On a LO, spurious signal will cause the desired output frequency to vary in phase at the IF frequency which creates an intermodulation process. Depending on the synthesizer application, some of the harmonics and spurious signal may or may not be a problem. Harmonic-cancelling sine-wave synthesis involves the weighted summation of a set of phase shifted square-waves to produce a step-wise sine-wave approximation [31].

Storch and Musch [32] have designed an ultralow-noise synthesizer with high spectral purity that is used in a time base of impulse radar system. The synthesizer uses the concept of frequency dividers with both short division factor sequence technique. It comprises a 5-bit programmable frequency divider with maximum input frequency of 2 GHz. A field programmable gate array (FPGA) is used to provide the required logic as well as to control the 14-bit DAC in the system.

A standard high speed flip-flop is used to perform the division by two processes. An ultra-low phase noise crystal oscillator working at 1 GHz frequency is used to provide the reference signal to the system. With this technique, the spurious free dynamic range (SFDR) has improved to 117dB which means no spurs are visible at signal frequency of 10.7 MHz. With the use of FPGA in the design, the advantage of having simplicity circuitry was obtained.

The inadequate spurious performance limitation of using a DDS synthesizer has lead Lesage, Capaine, Penn and Jestin [33] to the development of a wideband, low noise and low spurious agile frequency synthesizer based on the combination of surface acoustic wave (SAW) oscillator and high speed digital-to-analogue (DAC)

converter. The design uses a multiplied-frequency oven controlled SAW oscillator (OCSO) to provide the clock signal to the DAC and up-convert the output frequency of the DAC for any desired frequency band of interest.

At high frequency bandwidth, the synthesizer high spurious free dynamic range (SFDR) performance achieved was at -90 dBc respectively. However, the disadvantage of using this system is that it relies on a high linearity DAC performance which is expensive and costly.

A simple algorithm to counter the integer boundary spurs in a hybrid synthesizer was proposed by Vishnu and Anulal [34]. The developed algorithm has the capability of identifying if the frequency is prone to the integer boundary spurs or not. If it is, the output frequencies of the hybrid synthesizer are configured such that the generated spurs will be outside of the loop filter bandwidth and attenuated. A micro-controller is used to run the algorithm as a sub-routine for programming the hybrid synthesizer. To ensure sufficient spur suppression, the threshold was set at 2 MHz for the spur offset frequency. Any boundary spur within 2MHz on either side of the output frequency, the algorithm will suppress the spurs. However, this design still needs further improvement in terms of settling time and phase noise of the synthesizer.

2.6 Summary

This chapter has reviewed the work done by previous researches on hybrid synthesizers. It has been noted that characteristics like phase noise, switching speed and spectral purity of the output signal are the key parameters that need to be considered in determining the performance of a synthesizer. Among the reviewed method, none of them uses a PLL driven DDS concept in designing a hybrid synthesizer. Hence, this research will implement a hardware realization of the PLL driven DDS Hybrid Synthesizer and investigate the performance of the system. It is expected that the proposed system will have better phase noise performance due to the characteristic of the PLL that has low phase noise performance. Although some of the design covered in this chapter has its tradeoffs, but the ideas and concept discussed can be leverage in designing a promising high performance PLL driven DDS hybrid synthesizer for this study.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Overview

This chapter begins with the design of PLL driven DDS hybrid synthesizer used for this research. Section 3.2 will discuss more on the theory operation of the PLL. The following section of 3.3 will cover the DDS theory operation as well. Section 3.4 shows how the PLL and the DDS are combined to become a hybrid synthesizer. Section 3.5 will show how the phase noise is being measured. The switching speed measurement will be covered in section 3.6. Lastly, section 3.7 will discuss more on the method of measuring the spectral purity of the output signal produced by the hybrid synthesizer.